In-situ thermal annealing of CMOS devices after gamma irradiation

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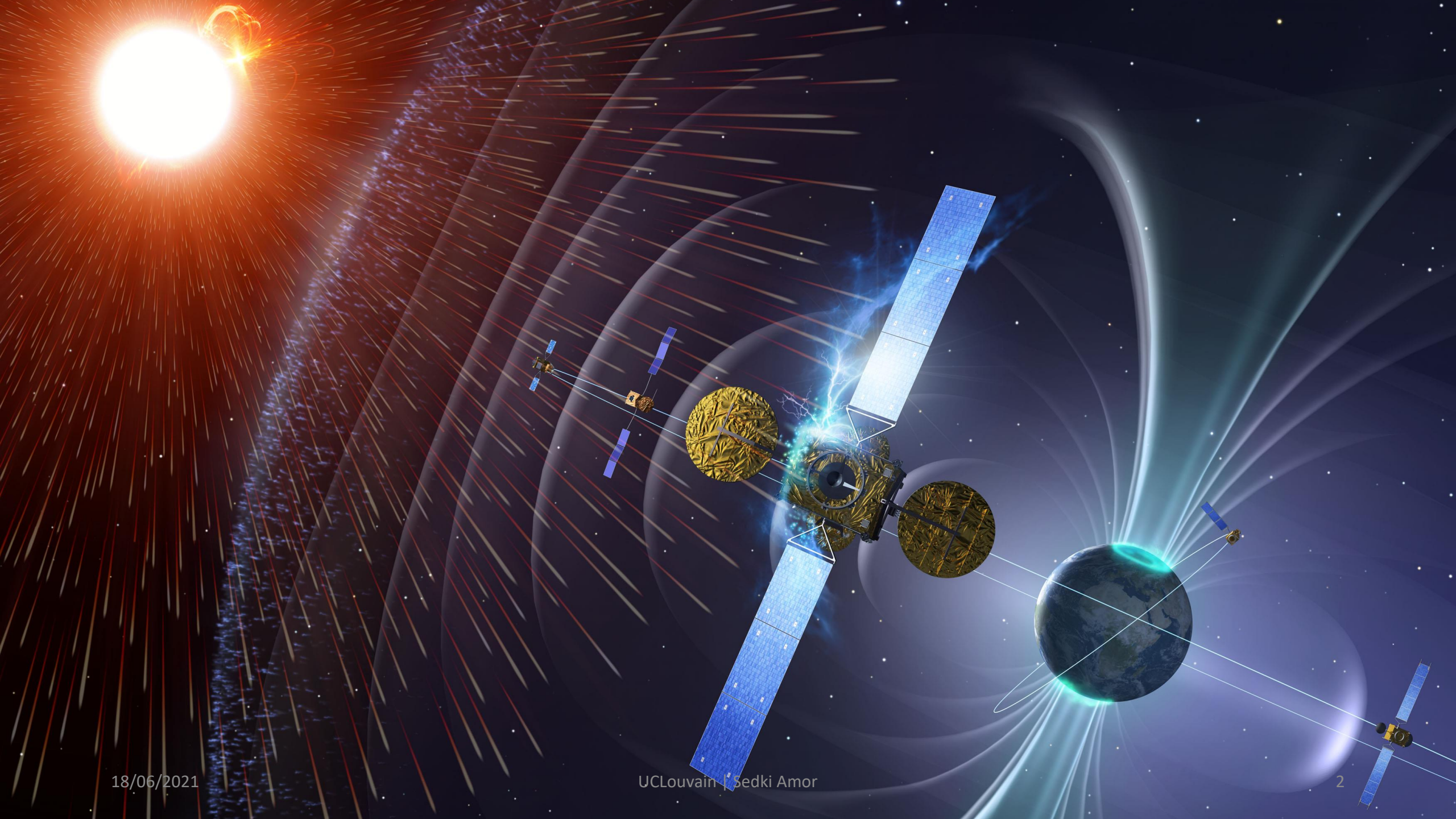
ICTEAM, UCLouvain.

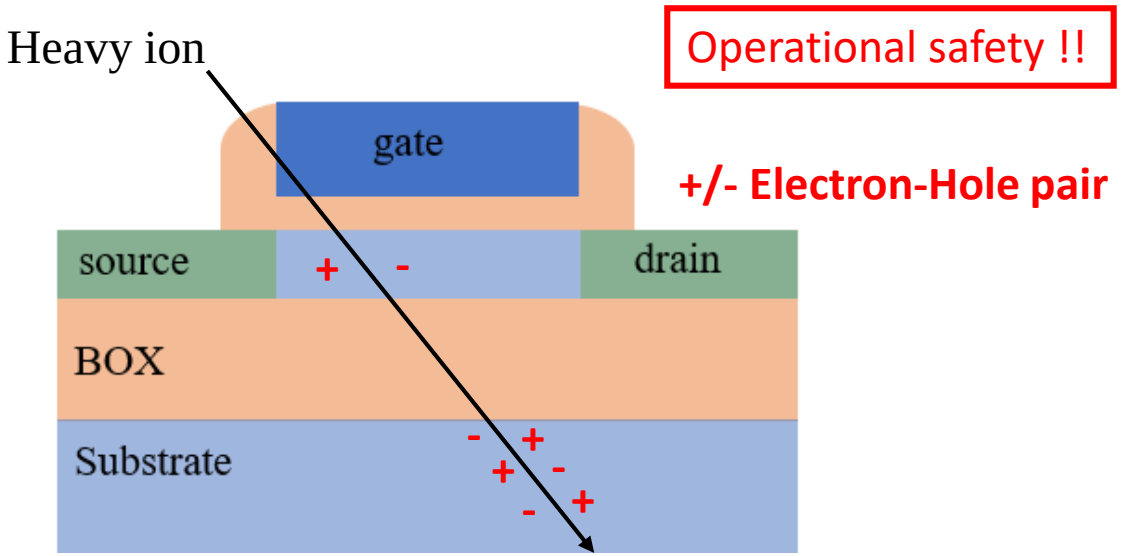


Outline

- Radiation-induced defects in SOI-based transistors.
- Device description.
- Measurement's setup for gamma irradiation.
- In-situ thermal annealing.
  - I-V measurements.
  - Low Frequency Noise Measurements.
- Perspective.
- Conclusion.

Radiation-induced defects in SOI MOSFETs

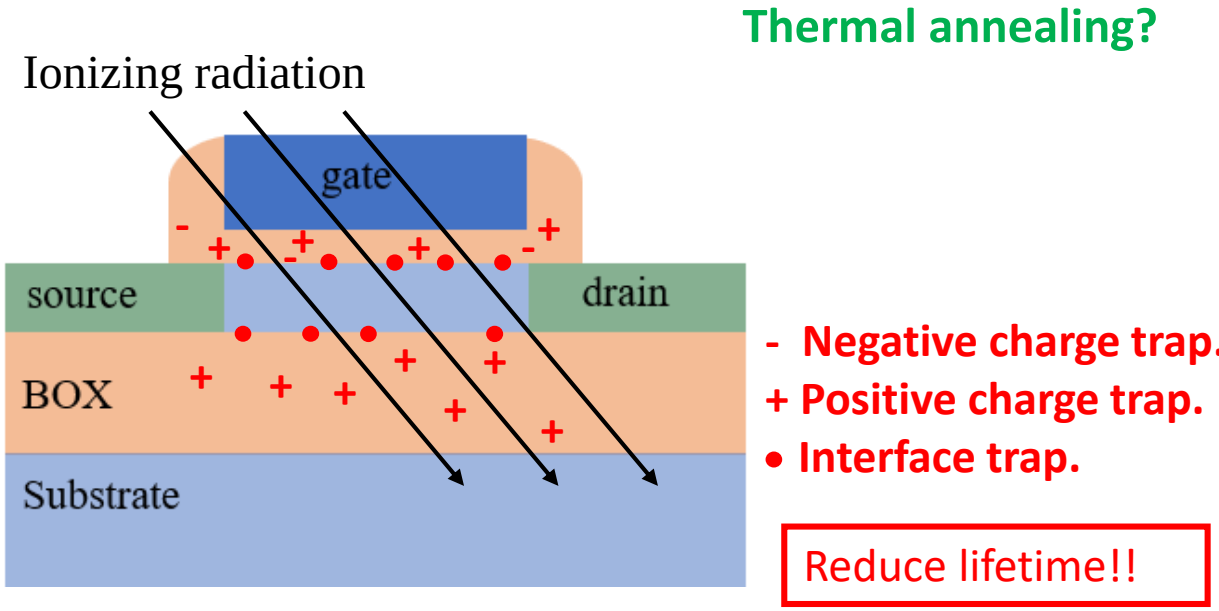
Single Event Effects



- SET : Transient
- SEU : Upset
- SEL : Latch-Up
- SEB : Burn- Out

- Insulation (SOI)
- Error Correction
- Duplex architecture
- Triple modular redundancy

Total Ionizing Dose



- Cumulative degradation
- Shift of parameters
- Permanent failure

- Shielding
- Rad-Hard design

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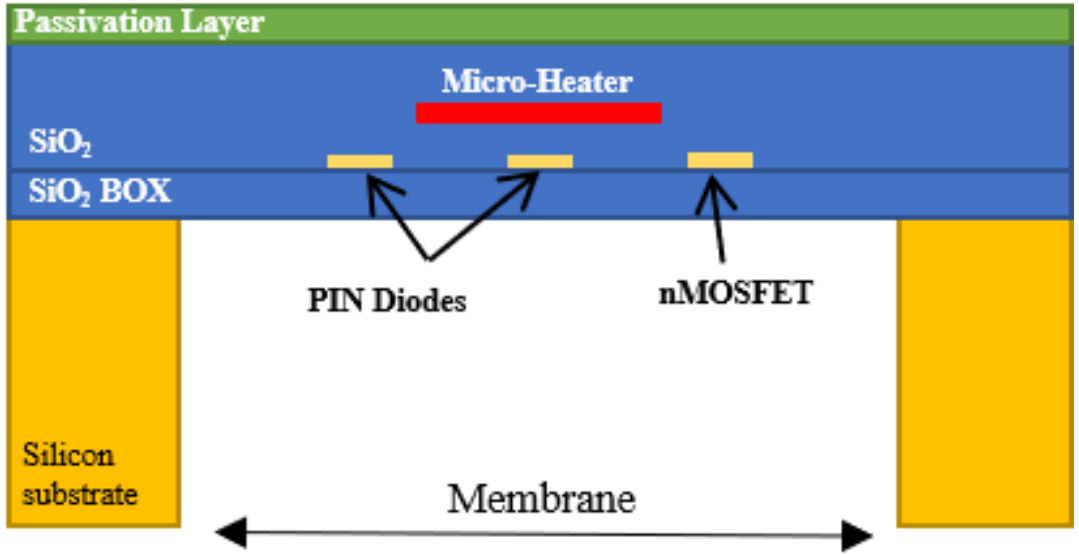
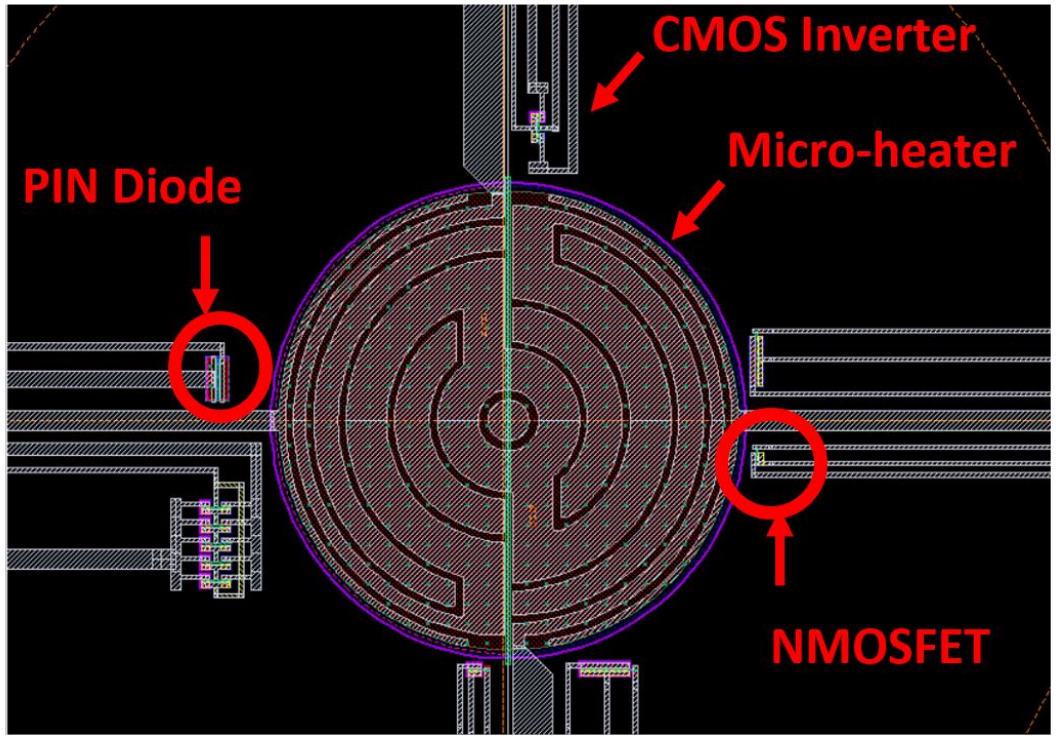
Device description.

The device has been fabricated using a 1.0 µm Partially-Depleted SOI technology (XI.10 from XFAB, Germany).

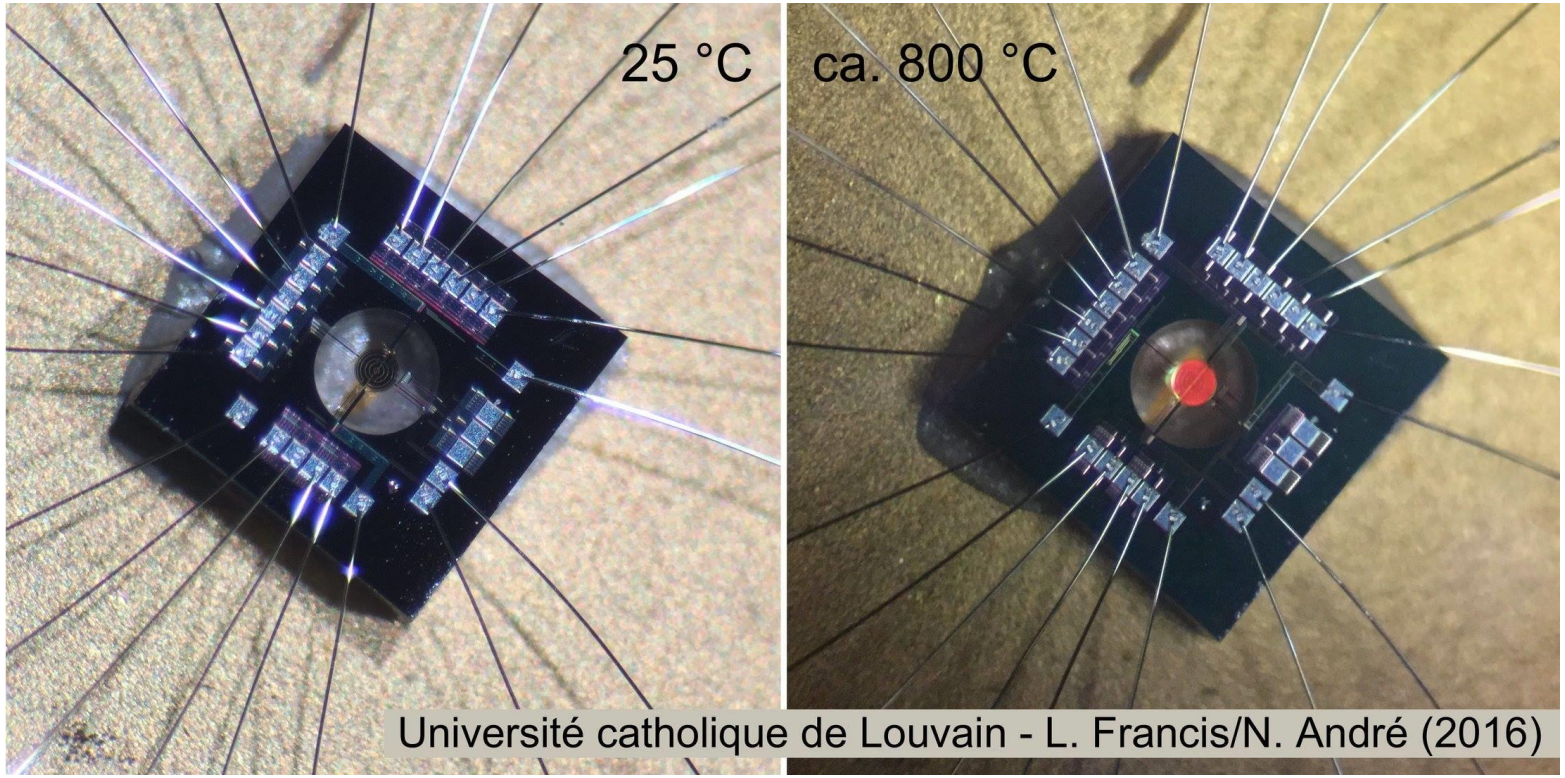


Schematic cross section of the device under test. (S Amor, et al, Semicond.Sci. and Techn., vol. 32, 2016.)

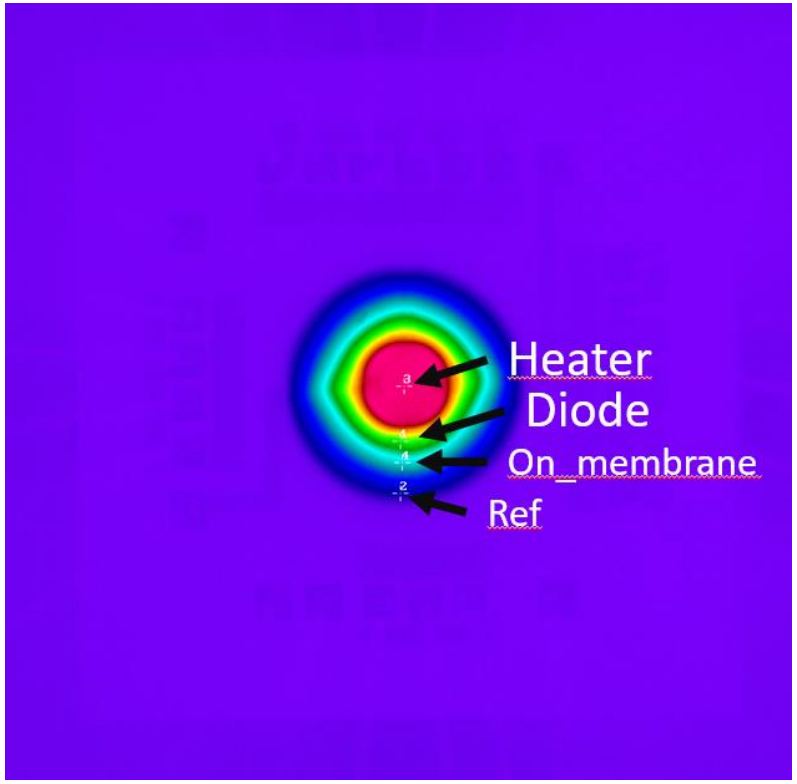


Layout image showing the location of the components around the micro-heater.

Device description.



Microscopic view of the device at a floating condition (Left) and under micro-heater biasing at 4V with maximum temperature of about 800 °C (right).



I-R camera shot of the device's front side.

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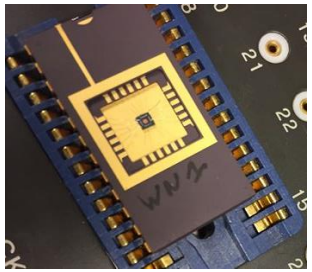
Measurement's setup for gamma irradiation

Cyclotron, Louvain-La-Neuve, Belgium.

Two Cobalt 60 sources with a dose rate of 1 krad/h (Si) each



Device Under Test wire-bonded in a DIL 24 ceramic package

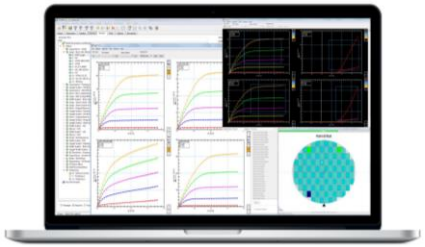
Total Dose 348 krad (Si) !!

Radiation room

Coaxial cables

HP 4156 Semiconductor Device Parameter Analyzer

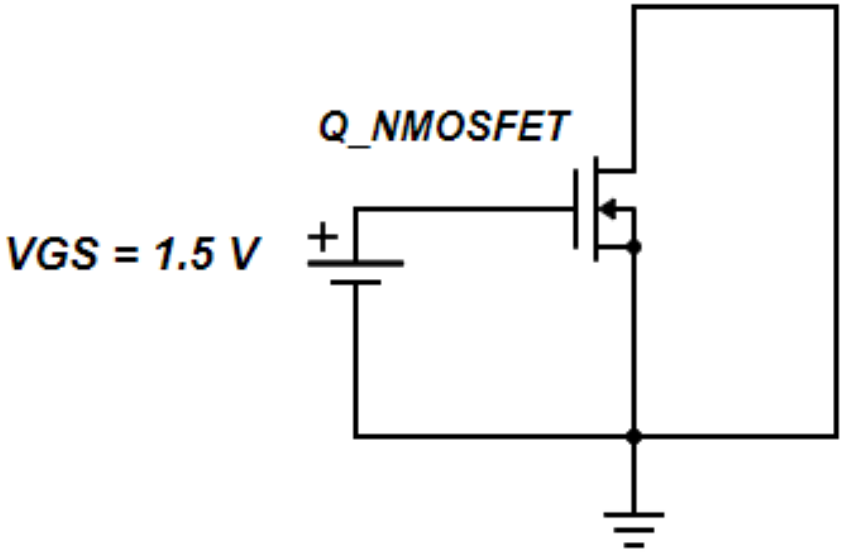
IC-CAP script Recall of a characterisation routine each 3 hours of exposure



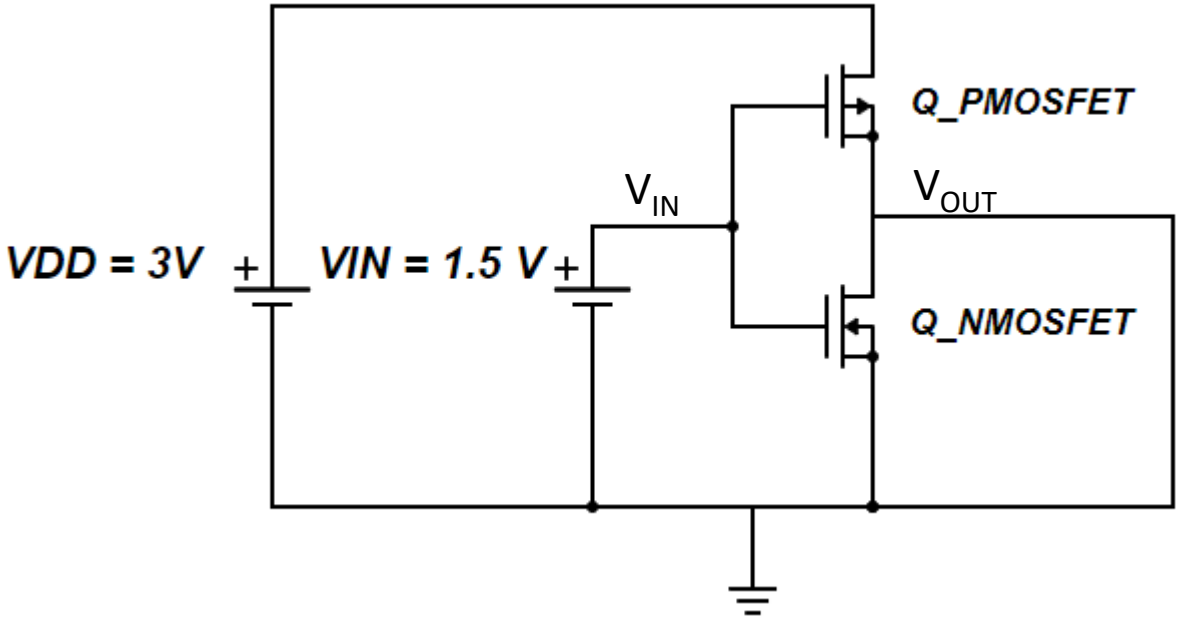
Armored room

Measurement's setup for gamma irradiation

Bias conditions at ionising radiation, increases the sensitivity to the total Ionizing Dose by separating electron-hole pairs in the gate-oxide !!



Bias condition of the 6µm wide transistor under gamma radiation.



Bias condition of the ON-membrane CMOS inverter. Designed by 4 µm wide N, and P-MOS transistors.

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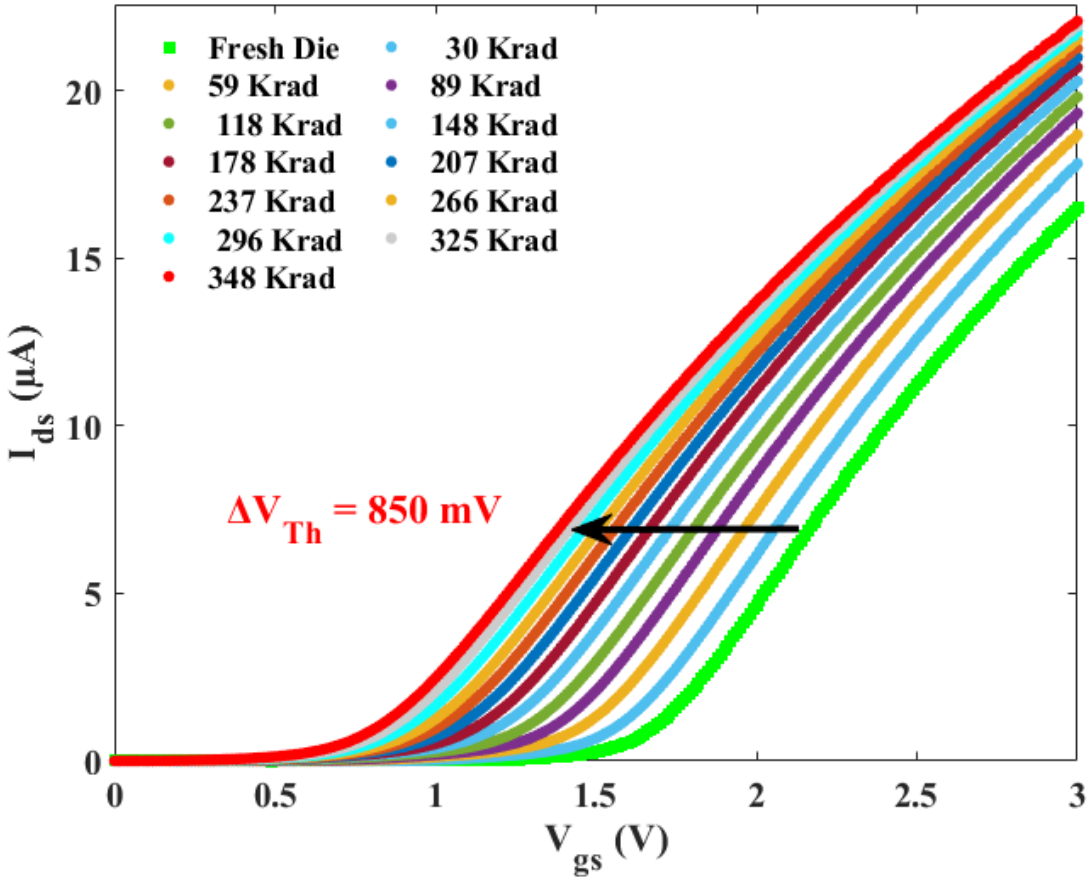
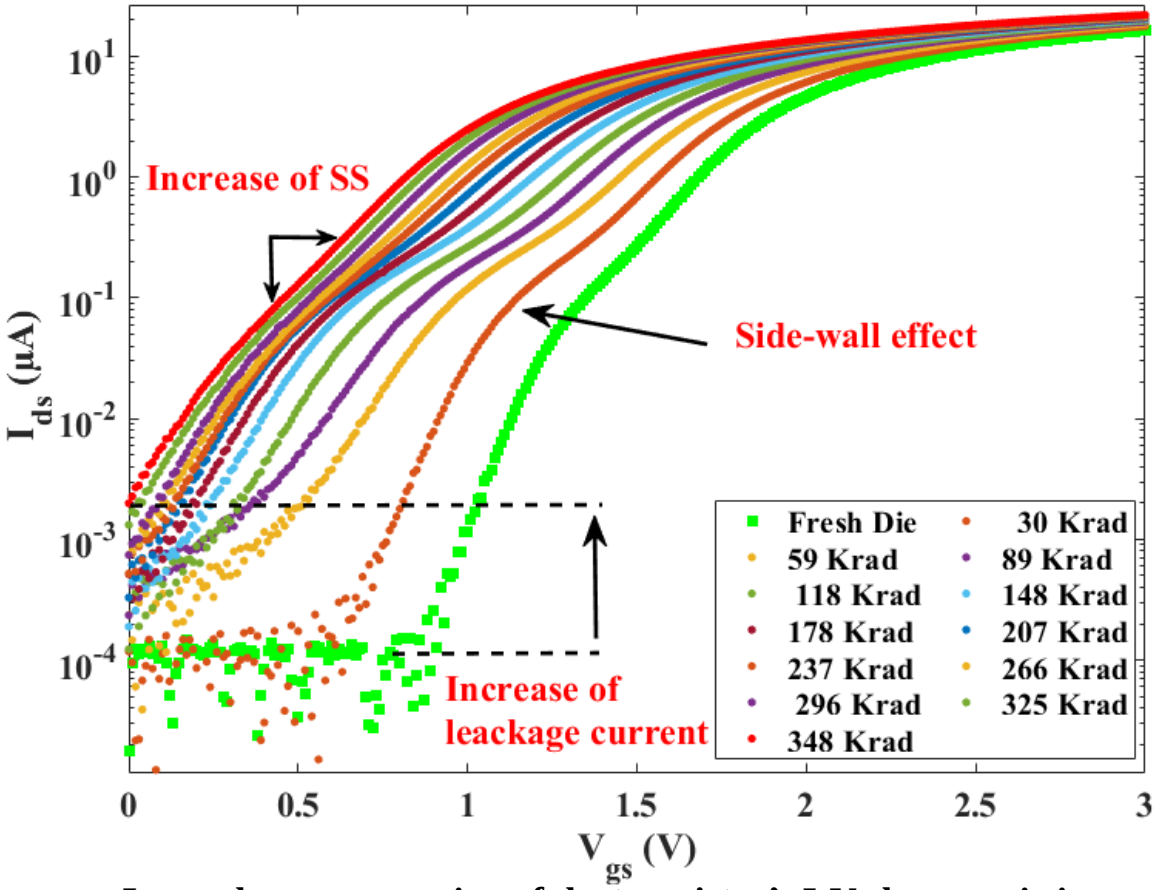
In-situ thermal annealing.

I-V characterization: During irradiation



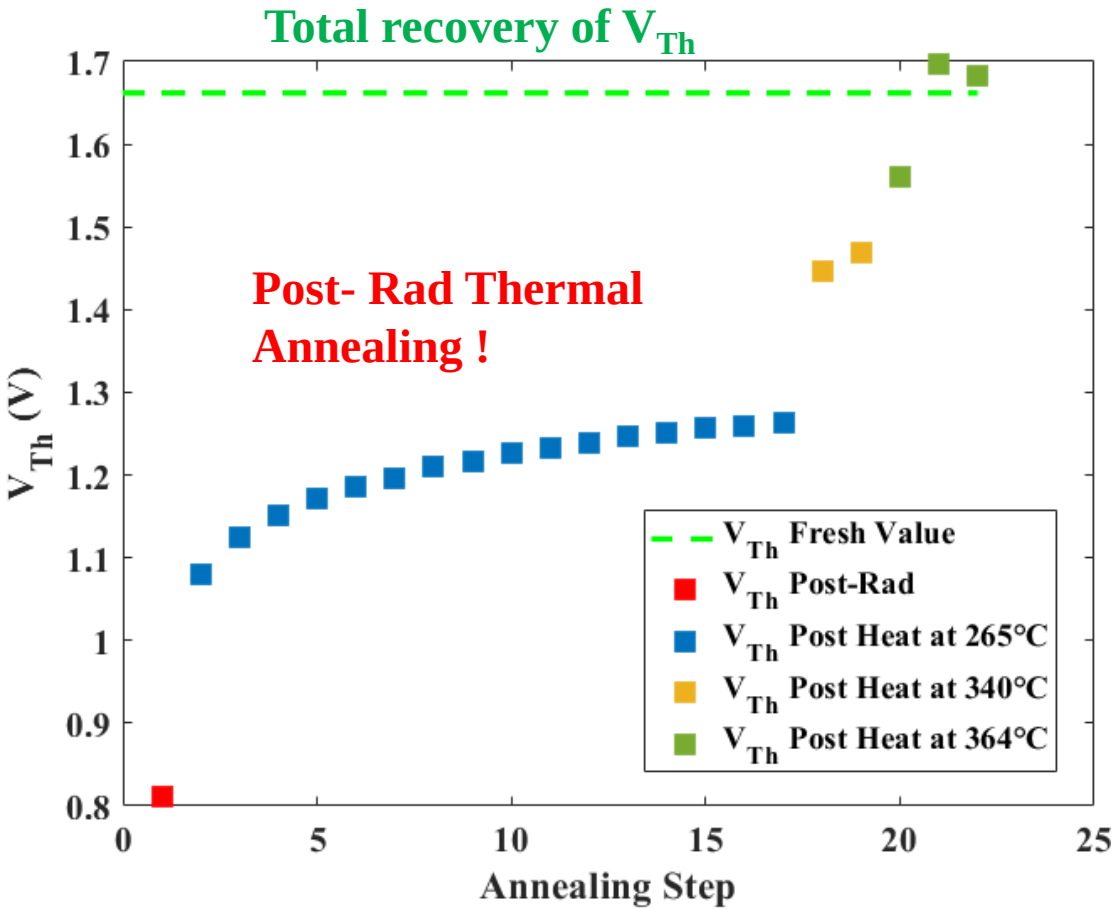
I_{ds} vs V_{gs} characteristics of the 6µm wide transistor. Measured in linear regime under after each 60 krad (Si) of gamma radiation .



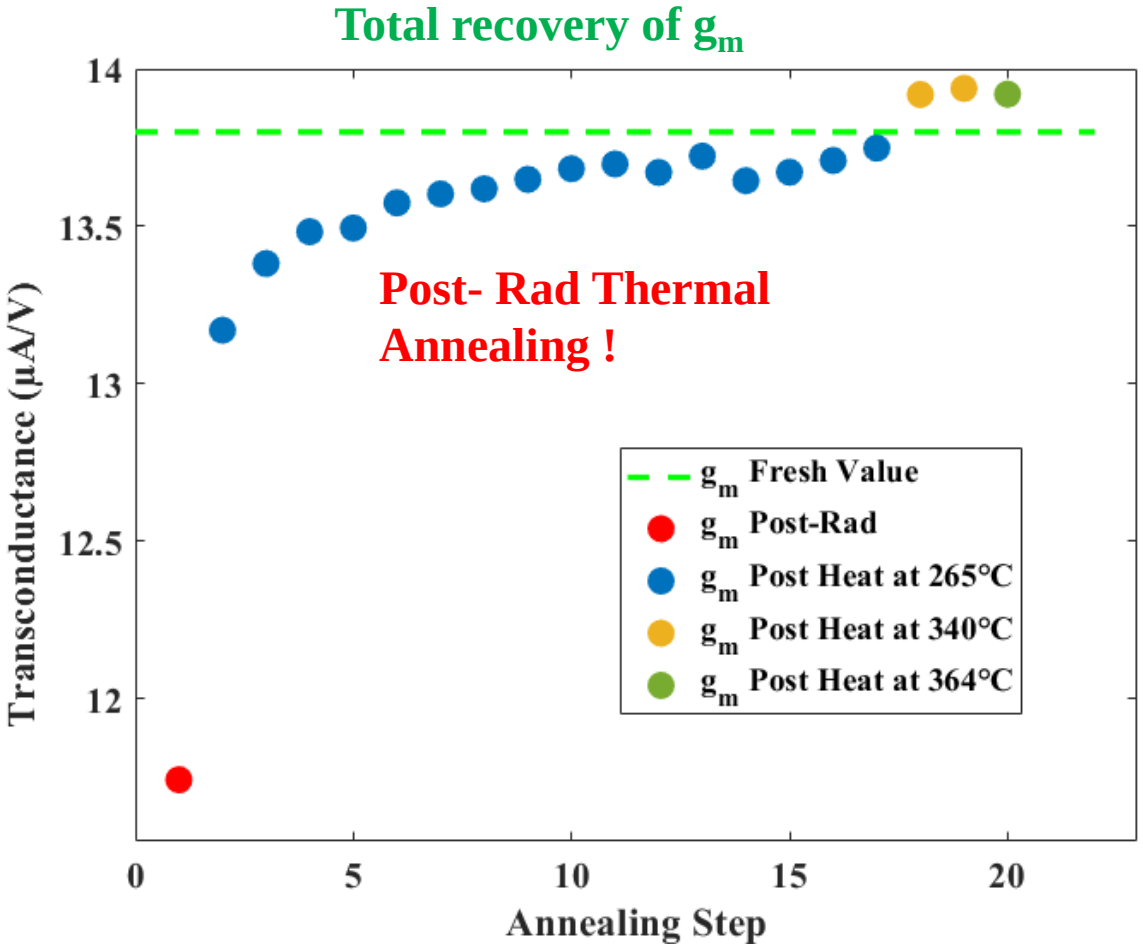
Logscale representation of the transistor's I-V characteristics. Measured under gamma radiation after each 60 krad (Si).

In-situ thermal annealing.

I-V characterization: Post-irradiation



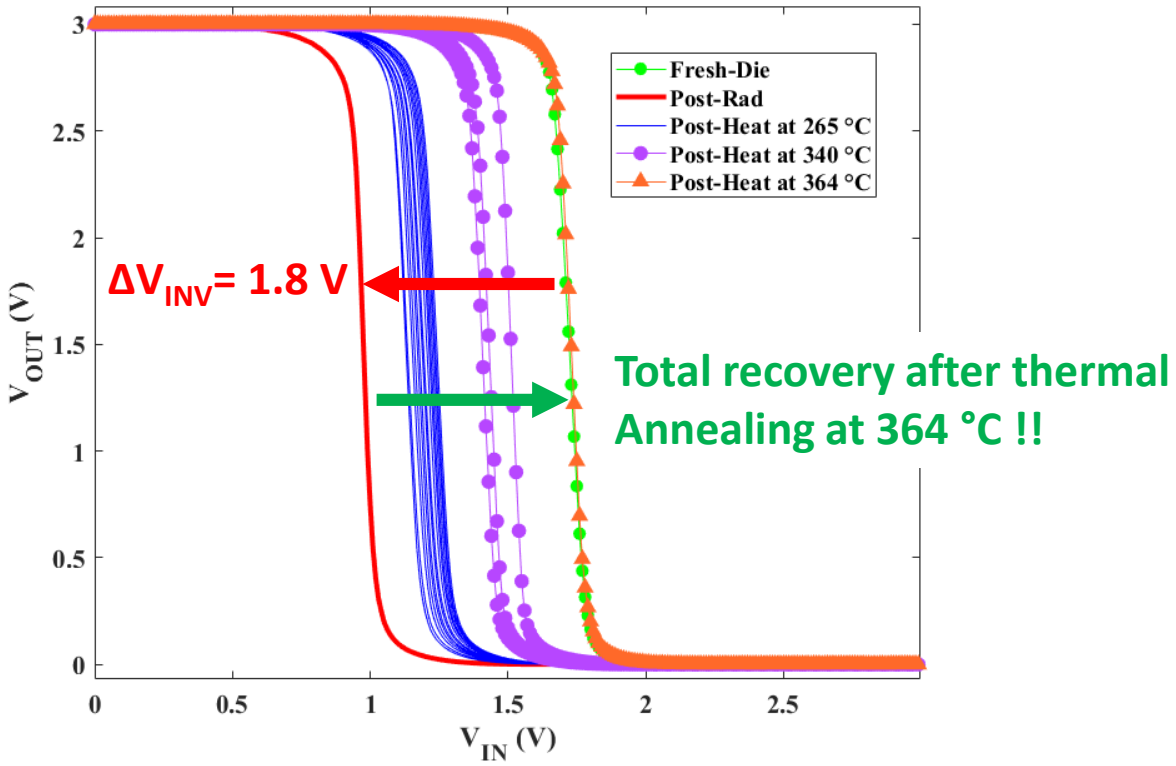
Threshold voltage of the transistor in fresh condition, after irradiation and after each annealing step.



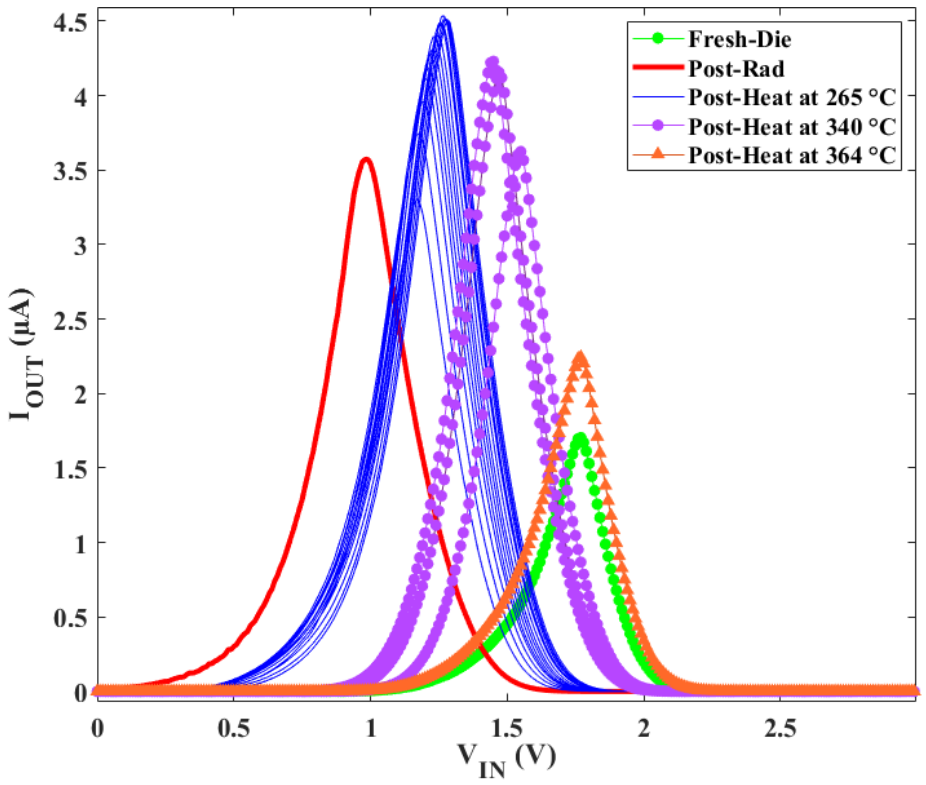
Maximum transconductance in linear regime, extracted in fresh condition, after irradiation and after each annealing step.

In-situ thermal annealing.

I-V characterization: Post-irradiation



Voltage transfer characteristics of the CMOS inverter after each annealing step



Output current of the CMOS Inverter measured after each annealing step

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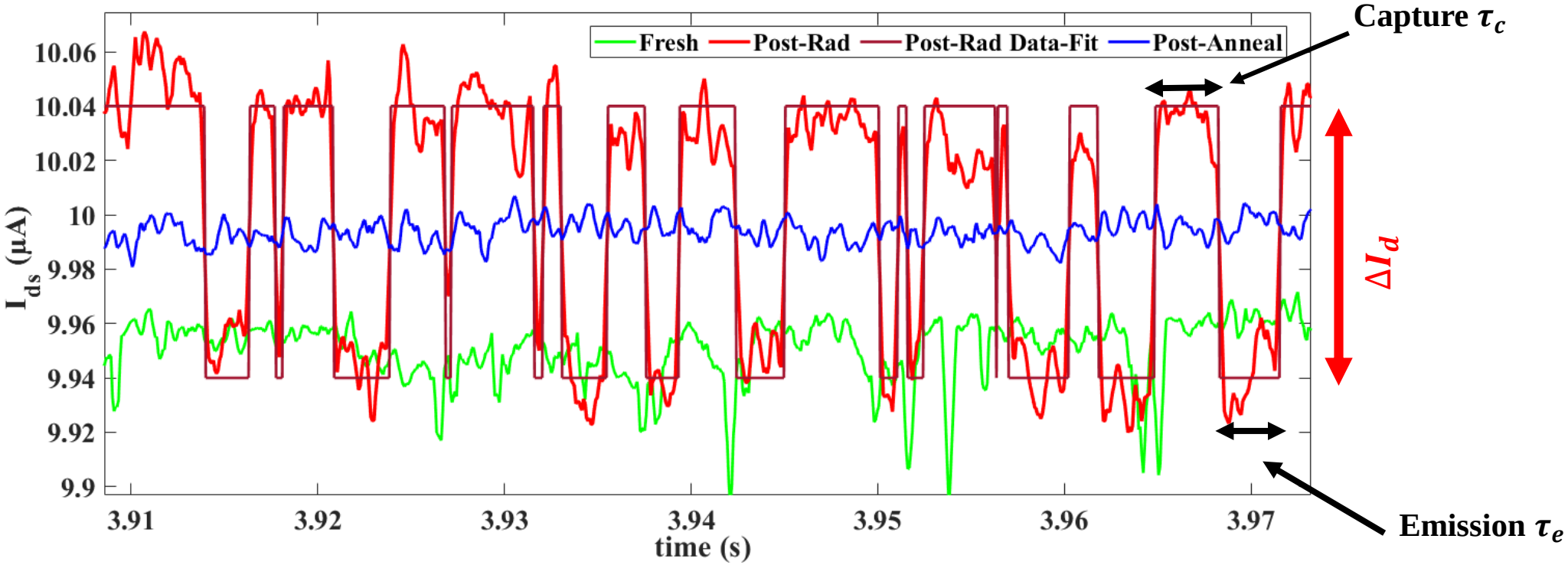
In-situ thermal annealing.

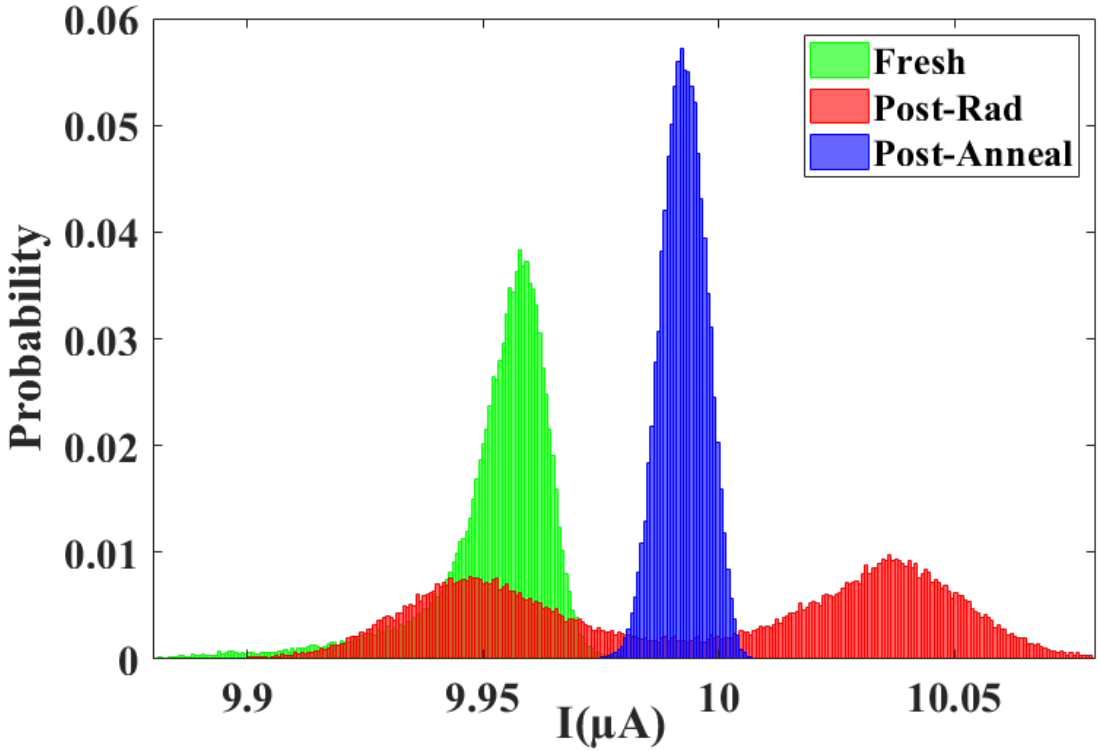
Low Frequency Noise measurements



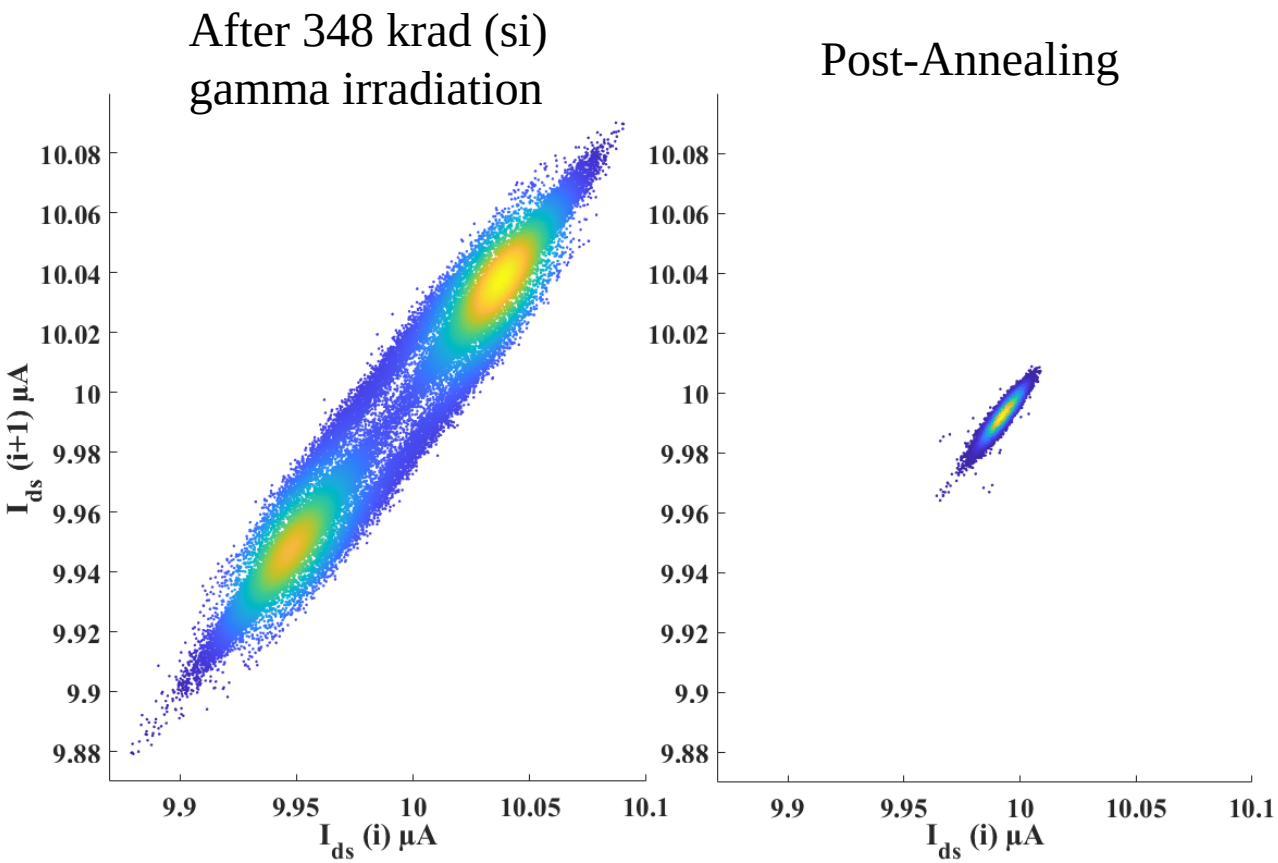
Time trace measurements I_d (t) Pre-Post Radiation and Post Annealing at fixed current I_{ds} = 10 µA with V_{ds} = 3 V.

In-situ thermal annealing.

Low Frequency Noise measurements



Probability distribution based on Time trace mesurements measured at fixed Ids= 10 µA and Vds= 3 V



Lag plot presentation of I_d (t) after irradiation and Post-annealing measured at fixed Ids= 10 µA and Vds= 3 V

In-situ thermal annealing.

Low Frequency Noise measurements

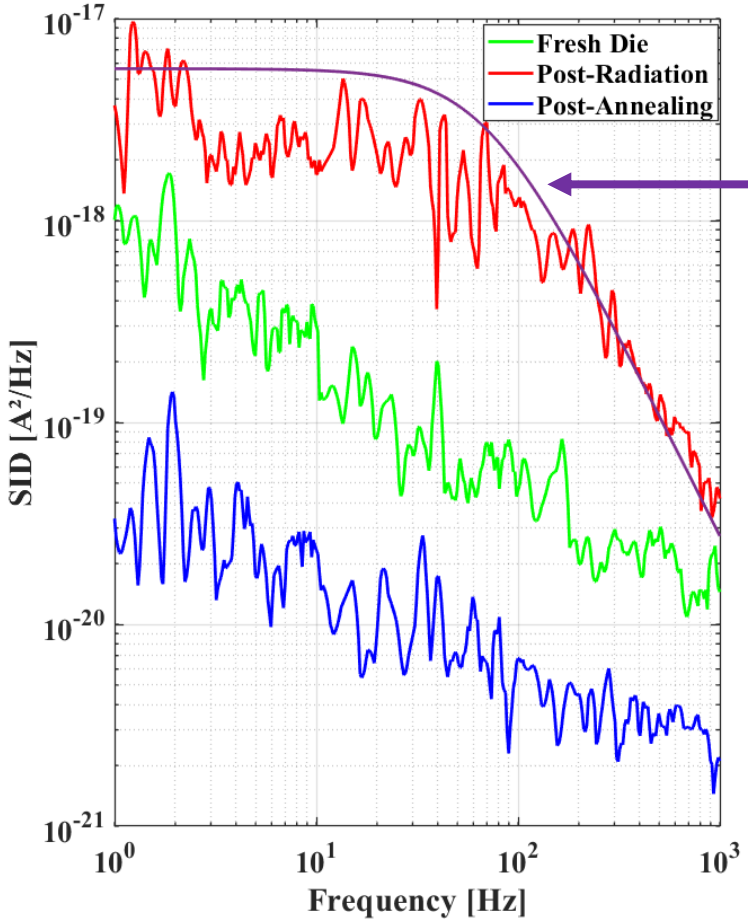
Lorentzian Model:

$$S_{id,RTN}(f) = \Delta I_d{}^2 \frac{4\,\tau^2}{\tau_e + \tau_c} \frac{1}{1 + (2\pi f \tau)^2}$$

where τ_e and τ_c refers to the emission and capture mean time constants and ΔI_d the current difference.

with

$$\frac{1}{\tau} = \frac{1}{\tau_e} + \frac{1}{\tau_c}$$



Lorentzian model based on the extracted time constants

Noise power spectral density of the MOSFETs. Measured Pre-Post radiation and after annealing at vds= 3 V.

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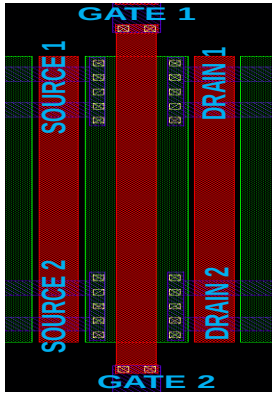
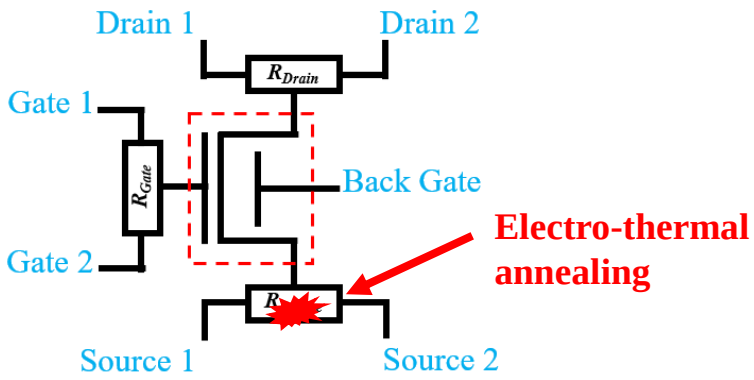
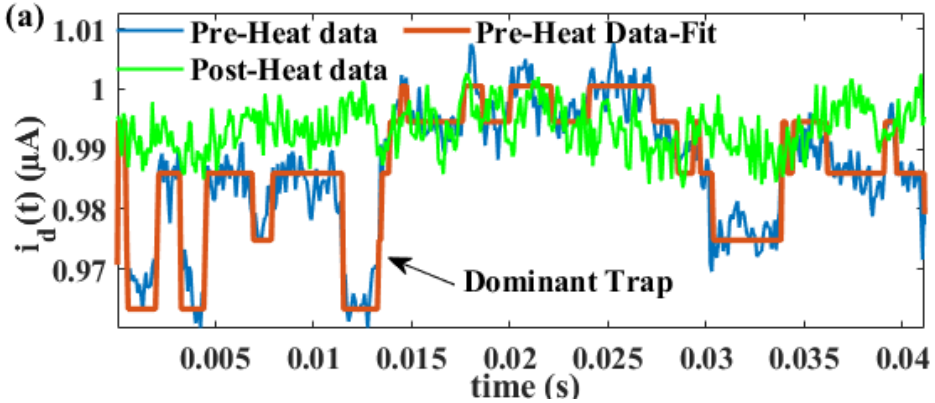
Perspective

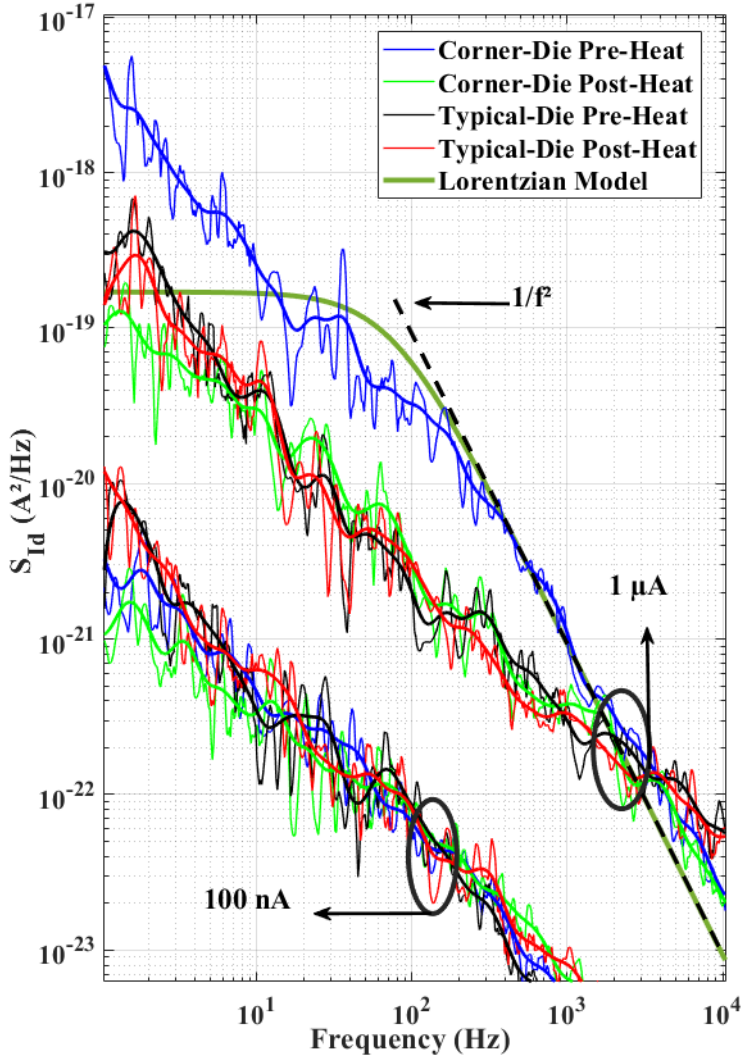




Layout of N-type MOS transistor with thick high-k metal gate oxide, from 28 nm Fully Depleted Silicon-On-Insulator (FDSOI) process.



Time trace measurements of the drain current of the fresh and post-heat Corner-Die in linear regime (V_d = 50 mV, with V_o = -50 mV).



Noise power spectral density of the MOSFETs. Measured before and after annealing in linear regime.
(S. Amor, et al, ,IEEE Electron Device Letters, 2021)

Conclusion

- In-situ Thermal annealing provided a total recovery of the transistor's electrical characteristics.
- Noise measurements provides advanced investigations of the oxide defects in MOSFETs.
- The time trace measurements I_d (t), confirmed the neutralisation of radiation-induced defects.
- Noise measurements demonstrated the reduction of 1/f noise after thermal annealing.